ABSTRACT OF THE DISCLOSURE

The present invention provides a compact electrostatic-breakdown-preventive and protective circuit for a semiconductor-device capable of performing high-speed operations. In the electrostatic-breakdown-preventive and protective circuit for a semiconductor-device of the invention, a protective transistor is provided between a power-source line and a ground line for an input/output circuit, a position between a power-source line and ground line for a circuit block A, a position between a power-source line and a ground line for a circuit block B, and a position between a power-source line and a ground line for an input/output circuit. A PMOS protective transistor is provided between the power-source line for the circuit block A and the power-source line for the circuit block B, and an NMOS protective transistor is provided between the ground lines in an internal-circuit region in the vicinity of a signal line (protective resistor).